Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-98 (Canceled).

99. (Original) A semiconductor device comprising:

a monolithic three dimensional array of charge storage devices formed in an amorphous or polycrystalline semiconductor layer over a monocrystalline semiconductor substrate; and

driver circuitry formed in the substrate at least in part under the array, within the array or above the array.

100. (Original) The semiconductor device of claim 99, wherein the driver circuitry comprises at least one of sense amps and charge pumps formed under the array in the substrate.

101. (Previously Presented) The semiconductor device of claim 99, wherein at least one surface between two successive device levels of the array is planarized by chemical mechanical polishing.

102. (Original) The semiconductor device of claim 101, wherein the array contains four or more device levels.

103. (Original) The semiconductor device of claim 102 wherein each charge storage device is selected from a group consisting of a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM, and a rail stack TFT EEPROM.

104. (Original) The semiconductor device of claim 103, wherein each level of array is separated from another level of the array by a polished planar interlayer insulating layer.

105. (Original) The semiconductor device of claim 104, wherein each device level is planar with respect to the adjacent device levels.

Claims 106-449 (Canceled).

450. (Previously Presented) A monolithic three dimensional array comprising a plurality of device levels containing charge storage devices disposed above a substrate, the array comprising:

a first layer of transition metal-crystallized silicon disposed above the substrate;

a p-n junction disposed in said first layer; and

a local charge storage film disposed adjacent to said first layer;

wherein the p-n junction comprises a junction between a source region and a channel or a drain region and a channel.

Claims 451-455 (Canceled).

456. (Previously Presented) A semiconductor monolithic three dimensional array of polycrystalline or amorphous charge storage devices comprising a plurality of device levels, wherein at least one surface between two successive device levels is substantially planar.

457. (Previously Presented) The array of claim 456, wherein the array contains four or more device levels.

458. (Previously Presented) The array of claim 457, wherein each charge storage device comprises a pillar TFT EEPROM.

459. (Previously Presented) The array of claim 457, wherein each charge storage device comprises a pillar diode with a charge storage region.

460. (Previously Presented) The array of claim 457, wherein each charge storage device comprises a self aligned TFT EEPROM.

461. (Previously Presented) The array of claim 457, wherein each charge storage device comprises a rail stack TFT EEPROM.

462. (Previously Presented) The array of claim 491, wherein the surface of an insulating or a conductive layer in each device level is planarized by chemical mechanical polishing.

463. (Previously Presented) The array of claim 491, wherein the surface of an interlayer insulating layer located between two levels is planarized by chemical mechanical polishing.

464. (Previously Presented) The array of claim 491, wherein a peak to peak roughness of the surface planarized by chemical mechanical polishing is 4000 Angstroms or less.

465. (Previously Presented) The array of claim 457, further comprising driver circuitry formed in the substrate at least in part under the array, within the array or above the array.

466. (Previously Presented) The array of claim 465, wherein the driver circuitry comprises at least one of sense amps and charge pumps formed under the array in the substrate.

Claims 467-474 (Canceled).

475. (Original) A semiconductor device comprising a monolithic three dimensional array of charge storage devices comprising a plurality of device levels, wherein at least one surface between two successive device levels has a peak to peak roughness of 4000 Angstroms or less within a stepper field.

476. (Original) The semiconductor device of claim 475, wherein the array contains four or more device levels.

477. (Original) The semiconductor device of claim 476, wherein each charge storage device comprises at least one of a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM and a rail stack TFT EEPROM.

478. (Original) The semiconductor device of claim 475, wherein the at least one surface between two successive device levels has a peak to peak roughness of 500 to 1000 Angstroms within a stepper field.

479. (Original) The semiconductor device of claim 478, wherein the at least one surface comprises a surface of an insulating or a conductive layer in each device level that is planarized by chemical mechanical polishing.

480. (Original) The semiconductor device of claim 478, wherein the at least one surface comprises a surface of an interlayer insulating layer located between two levels that is planarized by chemical mechanical polishing.

481. (Original) The semiconductor device of claim 475, further comprising driver circuitry formed in the substrate at least in part under the array, within the array or above the array.

482. (Original) The semiconductor device of claim 481, wherein the driver circuitry comprises at least one of sense amps and charge pumps formed under the array in the substrate.

483. (Previously Presented) The semiconductor device of claim 99, wherein the charge storage devices comprise non-volatile charge storage devices.

484. (Previously Presented) The semiconductor device of claim 99, wherein the array of charge storage devices is formed in a plurality of amorphous or polycrystalline semiconductor layers over the monocrystalline semiconductor substrate.

485. (Previously Presented) The semiconductor device of claim 484, wherein the plurality of amorphous or polycrystalline semiconductor layers comprise a plurality of amorphous or polycrystalline silicon layers.

486. (Previously Presented) The semiconductor device of claim 99, wherein the driver circuitry is formed in the substrate at least in part under the array.

487. (Previously Presented) The semiconductor device of claim 99, wherein the driver circuitry is formed within the array.

488. (Previously Presented) The semiconductor device of claim 99, wherein the driver circuitry is formed above the array.

489. (Previously Presented) The semiconductor device of claim 456, wherein the charge storage devices comprise non-volatile charge storage devices.

490. (Previously Presented) The semiconductor device of claim 456, wherein the array of charge storage devices is formed in a plurality of amorphous or polycrystalline semiconductor layers located over a monocrystalline semiconductor substrate.

491. (Previously Presented) The array of claim 456, wherein the at least one substantially planar surface between two successive device levels is planarized by chemical mechanical polishing.

492. (Previously Presented) The semiconductor device of claim 475, wherein the charge storage devices comprise non-volatile charge storage devices.

493. (Previously Presented) The semiconductor device of claim 475, wherein the array of charge storage devices is formed in a plurality of amorphous or polycrystalline semiconductor layers located over a monocrystalline semiconductor substrate.

494. (Previously Presented) The semiconductor device of claim 475, wherein the charge storage devices of the array comprise pillar TFT EEPROMs.

495. (Previously Presented) The semiconductor device of claim 475, wherein the charge storage devices of the array comprise pillar diodes with a charge storage region.

496. (Previously Presented) The semiconductor device of claim 475, wherein the charge storage devices of the array comprise self aligned TFT EEPROMs.

497. (Previously Presented) The semiconductor device of claim 475, wherein the charge storage devices of the array comprise rail stack TFT EEPROMs.

498. (Previously Presented) The semiconductor device of claim 497, wherein:

the array contains four or more device levels; and

the surface of an interlayer insulating layer located between two levels is planarized by chemical mechanical polishing.

499. (Withdrawn) A method of making a semiconductor device, comprising:

forming a plurality of device levels; and

planarizing at least one surface between two successive device levels by chemical mechanical polishing;

wherein:

the semiconductor device comprises a monolithic three dimensional array of charge storage devices comprising the plurality of device levels; and

the at least one surface between the two successive device levels has a peak to peak roughness of 4000 Angstroms or less within a stepper field.

500. (Withdrawn) The method of claim 499, further comprising:

forming four or more device levels; and

planarizing at least one surface between at least three successive device levels by chemical mechanical polishing.

501. (Withdrawn) The method of claim 500, wherein each charge storage device is selected from a group consisting of a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM, and a rail stack TFT EEPROM.

502. (Withdrawn) The method of claim 500, wherein a surface of an insulating layer in each device level is planarized by chemical mechanical polishing.

503. (Withdrawn) The method of claim 500, wherein a surface of a conductive layer in each device level is planarized by chemical mechanical polishing.

504. (Withdrawn) The method of claim 500, wherein the surface of an interlayer insulating layer located between two levels is planarized by chemical mechanical polishing.

505. (Withdrawn) The method of claim 500, further comprising forming driver circuitry in a substrate at least in part under the array, within the array or above the array.

506. (Withdrawn) The method of claim 505, wherein the driver circuitry comprises at least one of sense amps and charge pumps formed under the array in the substrate.

507. (Withdrawn) The method of claim 506, wherein the array of charge storage devices is formed in a plurality of amorphous or polycrystalline semiconductor layers located over a monocrystalline semiconductor substrate.